High-Performance V-Band Cascode HEMT Mixer and Downconverter Module

Junghyun Kim, *Student Member, IEEE*, Moon-Suk Jeon, Dongki Kim, Jinho Jeong, *Student Member, IEEE*, and Youngwoo Kwon, *Member, IEEE*

***Abstract*—A high-performance V-band cascode high electron-mobility transistor (HEMT) mixer is presented together with a compact downconverter module integrating the mixer with other receiver monlithic microwave integrated circuits (MMICs). The cascode mixer was optimized for conversion gain and/or linearity by employing the low-pass interstage networks and by optimizing the bias voltages. The low-pass interstage network effectively filters out the unwanted harmonics and spurious signals, and therefore, enhances the gain and the linearity of the cascode mixer. On a two-tone test, the cascode mixer showed a high conversion gain of 6.3 dB with an LO power of 2.6 dBm at 60 GHz. When the gate bias to the upper common-gate HEMT was tuned for the intermodulation distortion "sweet spot" theoretically predicted by the authors [1], the mixer showed a high third-order intecept point of 11.2 dBm with a decent gain of 4.1 dB under a small dc power consumption of 8 mW. To benchmark the performance of the cascode mixer of this work, a waveguide-based compact V-band downconverter module was built by integrating the mixer with an MMIC low-noise amplifier, a voltage-controlled oscillator, and an local oscillator (LO) driving amplifier. Thanks to the high gain and the on-chip RF/LO combining capability of the cascode mixer, a compact downconverter module was realized without a coupler and an IF amplifier. The downconverter module showed a conversion gain higher than 20 dB from 57.5 to 61.7 GHz. This paper shows the potential of the cascode FET mixer for high-performance compact downconverter applications at millimeter-wave frequencies.**

***Index Terms*—Downconverter, high conversion gain, linearity, millimeter-wave, V-band cascode mixer.**

I. Introduction

AMONG various mixer types using FETs, dual-gate FET (DG-FET) type mixers including cascode-connected mixers are of particular interest for monolithic applications. DG-FETs offer on-chip RF/local oscillator (LO) combining capability using the two isolated gates as LO and RF ports. DG-FET mixers also provide the possibility of conversion gain [2]. In this way, the need for bulky couplers and IF amplifiers can be eliminated, resulting in a small die size. Most DG-FET type mixers have so far been realized at low frequencies such as the L-band, which have shown desirable conversion gain and intermodulation distortion (IMD) characteristics [3]–[5]. On the other hand, millimeter-wave applications of dual-gate or cascode mixers have been very limited compared with other types of FET mixers and diode mixers [6]–[8]. One exception is a W-band dual-gate high electron-mobility transistor (HEMT) mixer reported by one of the authors [9]. The W-band mixer employed dual-gate InP-based HEMTs and showed a conversion loss of 3 dB at 94 GHz. Recently, a balanced HEMT gate mixer has been reported at 50 GHz, which showed a high conversion gain of 8 dB [10]. However, bulky on-chip couplers and external IF baluns were needed for operation [10], making it unsuitable for compact downconverter applications.

This paper presents a high-performance monolithic GaAs cascode HEMT mixer for compact downconverter applications at the V-band. The mixer was realized in a small chip size of 1.6×1.6 mm^2 including all the matching circuits as well as on-chip RF/LO coupling. It showed a high conversion gain of 6.3 dB when tuned for conversion gain and presented a high third-order intercept point (IP3) of 11.2 dBm when tuned for linearity. To the best of our knowledge, a gain of 6.3 dB is among the highest conversion gains in this frequency range.

In order to demonstrate the usefulness of the cascode mixer for compact downconverter applications, a low-cost V-band downconverter module was built using the cascode HEMT mixer of this work. Measured RF conversion gains of the reported downconverters were limited at frequencies above the V-band due to the high loss of the mixer [7], [11]. Therefore, additional IF amplifiers were needed at the end of the receiver to boost the overall conversion gain [6]. In this work, a compact V-band downconverter module has been demonstrated using the high-gain cascode mixer, showing conversion gains higher than 20 dB from 57.5 to 61.7 GHz without using IF amplifiers.

Detailed design methods to achieve high gain as well as good linearity are shown in Section II, followed by the measured results in Section III. The construction and measured results of the V-band downconverter using the mixer of this work are shown in Section IV.

II. Design of V-Band Cascode FET Mixer

The goal of this study was to optimize the design of a V-band cascode FET mixer to achieve high conversion gain and linearity. This was achieved by employing interstage matching networks and optimizing bias conditions. Fig. 1 shows the equivalent-circuit schematic of a cascode FET mixer as represented by a stack of common-source (CS) and common-gate (CG) FETs. Also shown in Fig. 1 are the matching circuits used in this work. As shown in our previous work [1], mixing and IMD generation occurs mostly in the lower FET (CS-FET), which operates like a drain-pumped mixer. The upper CG-FET, on the other hand, operates as a source follower, providing LO pumping to the lower FET. It also works as a CG IF postamplifier and mixer, in

Manuscript received December 14, 2001; revised October 8, 2002. This work was supported by the Korean Ministry of Science and Technology under the Creative Research Initiative Program.

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Digital Object Identifier 10.1109/TMTT.2003.808612

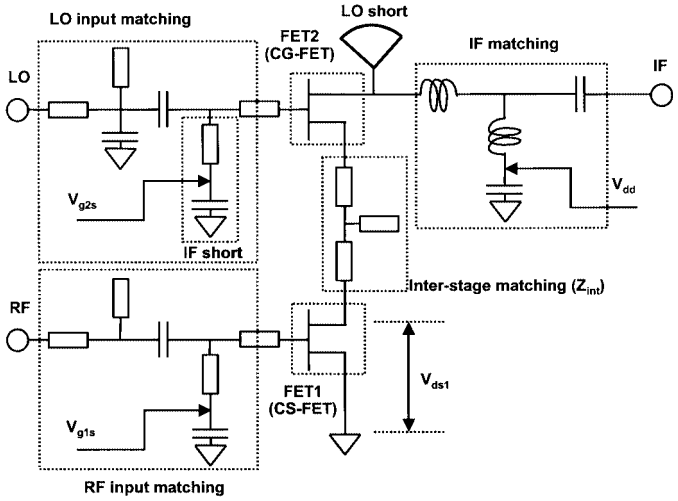

Fig. 1. Equivalent=circuit schematic of a cascode mixer.

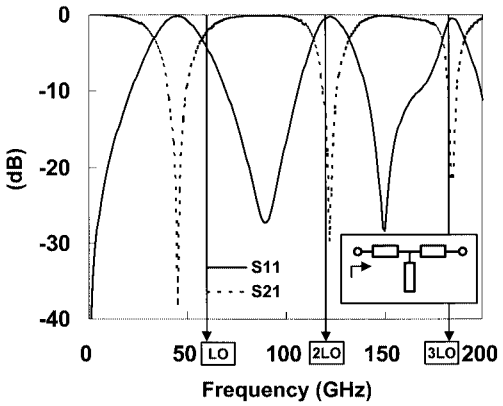

Fig. 2. Simulated $S11$ and $S21$ of the interstage matching network of mixer A.

which case the higher order mixing products from the CG-FET complicates overall IMD characteristics. Generally, the lower CS-FET is connected directly to the upper CG-FET without any interstage circuits. Thus, various harmonics and spurious signals generated by the lower CS-FET are fed to the upper CG-FET without any filtering. As has been theoretically demonstrated in our previous work [1], these harmonics and spurious signals can degrade the conversion gain as well as the linearity. In this work, we have employed an interstage circuit between the two transistors ($Z_{\rm int}$ in Fig. 1) to filter out the spurious signals, thereby improving gain and linearity. The interstage circuit is basically a low-pass filter structure with periodical band-reject characteristics near the harmonics of RF and LO frequencies to effectively prevent the harmonics generated in the lower CS-FET from being injected into the upper CG-FET. In order to clarify this, the S-parameters of the interstage matching network have been simulated and are shown in Fig. 2. The interstage network passes the IF frequency components while blocking the harmonics of RF and LO. For the LO signals, it also works as a reactive matching circuit, providing proper match to reduce reflections. Higher conversion gain with a lower LO power requirement is thus expected. This approach is applicable to the frequency ranges where one can easily realize a low-pass interstage network with proper rejection to the harmonics.

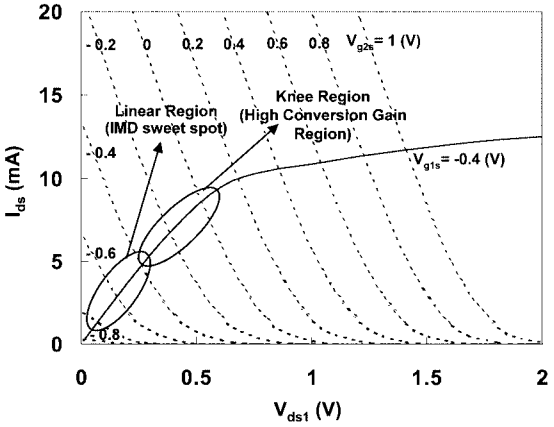

Fig. 3. I–V characteristics of a cascode-connected FET at a fixed V_{g1s} of -0.4 V. Depending on V_{g2s}, two different operating regions of interest can be found, as denoted with circles.

In addition to the introduction of interstage matching circuits, bias optimization was performed to enhance the gain and/or linearity. The gate bias to the lower FET (V_{g1s} in Fig. 1) determines the overall gain, current, and stability of the cascode mixer; V_{g1s} biased for maximum transconductance (G_m) of the CS-FET results in high conversion gain. The gate bias to the upper FET (V_{g2s} in Fig. 1) determines the operating point on the I_{ds}–V_{ds1} curve of the lower FET as illustrated in Fig. 3. Thus, V_{g2s} is expected to have strong effects on the transconductance, output conductance, and their derivatives. As presented in [1] and [2], a V_{g2s} bias choice can result in either conversion gain- or linearity-optimized mixers provided proper circuit design is followed; "knee bias" ($V_{g2s} \sim -0.3$ V) results in a high conversion gain while "linear bias" ($V_{g2s} \sim -0.6$ V) just outside the knee region allows optimum linearity, as well as a lower return loss of the LO port, corresponding to the IMD "sweet spot." This kind of mixer can be unstable by setting V_{g1s} to high gain bias and simultaneously choosing V_{g2s} near or above the knee bias [2]. In order to guarantee that the mixer operates at its best under the two V_{g2s} bias regions of interest while avoiding stability problems, V_{g1s} was chosen to be slightly below the maximum G_m point (-0.4 V).

III. Measured Results of a V-Band Cascode HEMT Mixer

V-band cascode HEMT mixers were designed with the aforementioned concepts and analyzed with the analysis method developed by the authors in [1]. Two types of cascode HEMT mixers were fabricated to demonstrate the circuit concept. One circuit (referred to mixer A) was designed with the proper interstage matching network ($Z_{\rm int}$ in Fig. 1) and, for comparison, the other one (mixer B) was designed without any interstage matching networks. Both mixers used identical transistors with a gate length of 0.15 μm and a width of 80 μm. Commercial GaAs pseudomorphic high electron-mobility transistor (pHEMT) foundry was used for chip fabrication. Fig. 1 shows the equivalent-circuit schematic of the V-band cascode mixers. The gate bias network included a $\lambda/4$ transmission line terminated with a large capacitor for IF short and an IF

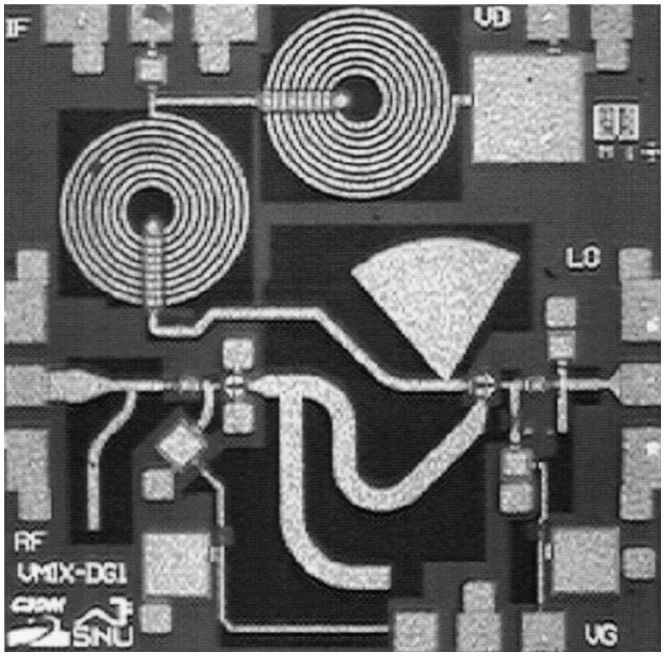

Fig. 4. Photograph of the miniaturized V-band cascode FET mixer (chip size: 1.6×1.6 mm^2.

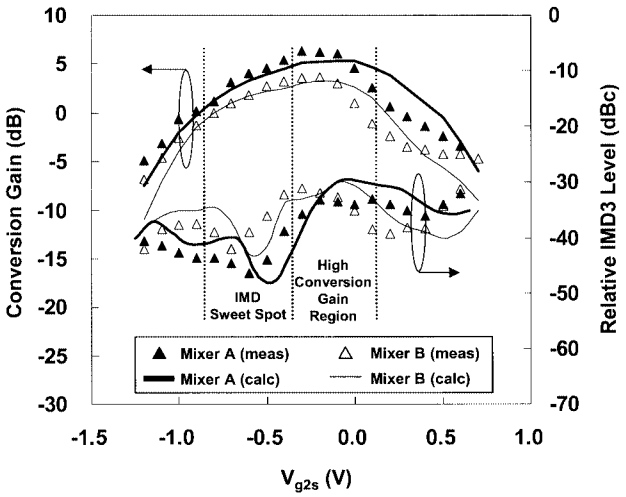

Fig. 5. Calculated and measured conversion gain and relative IMD3 level of V-band cascode FET mixers at a fixed V_{g1s} of -0.4 V and V_{dd} of 2.5 V. The RF input power is -16.1 dBm and the LO power is 2.6 dBm.

matching circuit consisting of spiral inductors and MIM capacitors was included on-chip. The photograph of the fabricated chip (mixer A) is shown in Fig. 4. The die size is 1.6×1.6 mm^2 including interstage, RF, and IF matching circuits.

The mixer chip was first tested for conversion gain and IMD using on-wafer probe station. The frequencies of the two-tone RF signals were 60.3 and 60.31 GHz and the LO frequency was 59.3 GHz, resulting in IF signals at 1000 and 1010 MHz and third-order IMD (IMD3) signals at 990 and 1020 MHz. Fig. 5 shows the calculated and the measured conversion gain and relative IMD3 levels of the V-band mixer as a function of V_{g2s} at a fixed V_{g1s} of -0.4 V and V_{dd} of 2.5 V. RF input power was -16.1 dBm and LO power was 2.6 dBm. As predicted by the theory, the conversion gain was highest near

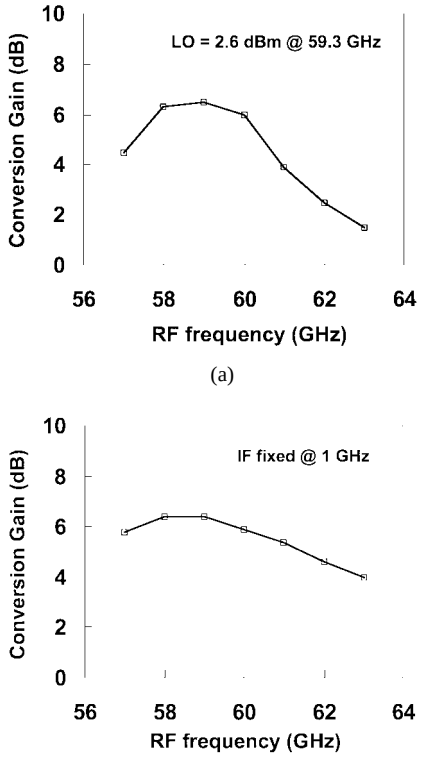

Fig. 6. Measured conversion gain of the V-band cascode FET mixer as a function of the RF frequency (a) at a fixed LO frequency of 59.3 GHz and (b) at a fixed IF frequency of 1 GHz.

the knee bias ($V_{g2s} \sim -0.3$ V) and the IMD "sweet spot" was clearly observed near $V_{g2s} \sim -0.6$ V. Also, mixer A (with interstage circuit) showed higher conversion gain and better IMD characteristics compared with mixer B. Biased for best gain region, the conversion gain increased by 2.7 dB, from 3.6 dB for mixer B to 6.3 dB for mixer A. Biased at the IMD "sweet spot," IMD3 levels were reduced by more than 5 dB for mixer A compared to mixer B. To the best of our knowledge, 6.3-dB gain is among the highest conversion gains reported in this frequency range. The measured IMD results suggest that excellent intermodulation characteristics (IMD3 of 46.4 dBc) can be achieved with a reasonable conversion gain (4.1 dB) when the mixer is bias tuned for the IMD "sweet spot." Fig. 5 also shows good correspondence between the measurement and simulation for both conversion gain and IMD characteristics. The corresponding output third-order intercept point (OIP3) was as high as 11.2 dBm with a low dc power consumption of 8 mW.

Fig. 6 shows the measured RF frequency dependence of the conversion gain of the cascode mixer. Fig. 6(a) shows the conversion gain as a function of the RF frequencies with a fixed LO source (frequency $=$ 59.3 GHz, power $=$ 2.6 dBm). It shows a 3-dB RF bandwidth of 4 GHz (57–61 GHz) under the fixed LO conditions. Fig. 6(b) shows the RF frequency dependence with the fixed IF frequency of 1 GHz. The mixer showed a conversion gain higher than 4 dB over a wider RF bandwidth from 56 to 62 GHz, demonstrating that the RF bandwidth is rather limited by the bandwidth of the IF matching circuit more than that of the RF matching circuit.

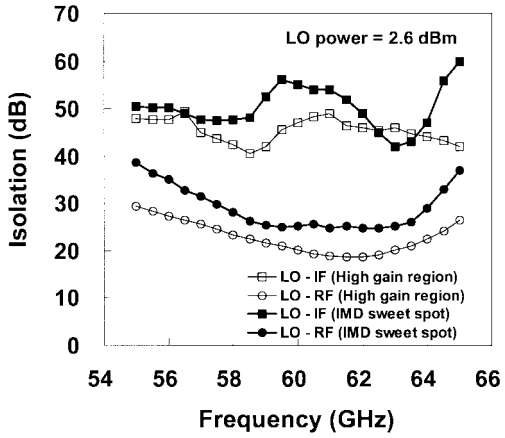

Fig. 7. Measured LO-to-RF and LO-to-IF isolation characteristics of the V-band cascode FET mixer.

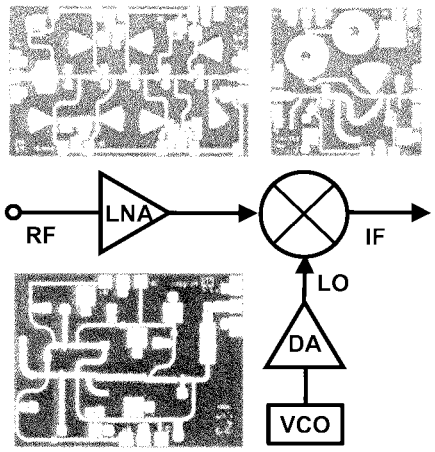

Fig. 8. Schematic of the overall integrated V-band downconverter module and the photographs of the individual chips.

The measured small-signal return losses at the RF and LO ports are typically −12 and −9 dB, respectively. The measured small-signal return loss data were not shown in this paper. Port-to-port isolation characteristics were also measured at a fixed LO power of 2.6 dBm and are shown in Fig. 7 for the two different V_{g2s} bias points. LO-to-RF isolation was higher than 20 dB, and LO-to-IF isolation was above 40 dB over the entire pass band, demonstrating excellent isolation characteristics.

IV. V-Band Downconverter Module

In order to demonstrate the usefulness of the cascode mixer in realizing compact downconverters at the V-band, a low-cost downconverter module was built using the cascode HEMT mixer of this work. For this purpose, a low-noise amplifier (LNA), a voltage-controlled oscillator (VCO), and an LO driving amplifier (DA) were integrated together with the cascode mixer of this work in a waveguide-based package. All these circuits were designed by the authors at Seoul National University and fabricated using the aforementioned 0.15-μm GaAs pHEMT commercial foundry ($f_T \sim 75$ GHz, $f_{\max} \sim 180$ GHz). The schematic of the V-band downconverter is shown in Fig. 8 along with the photographs of each chip.

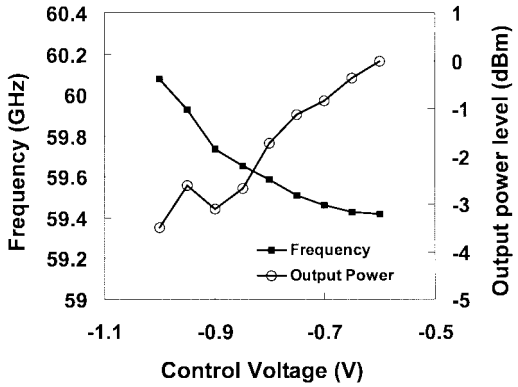

Fig. 9. Dependence of the oscillation frequency and power on the control bias of the VCO.

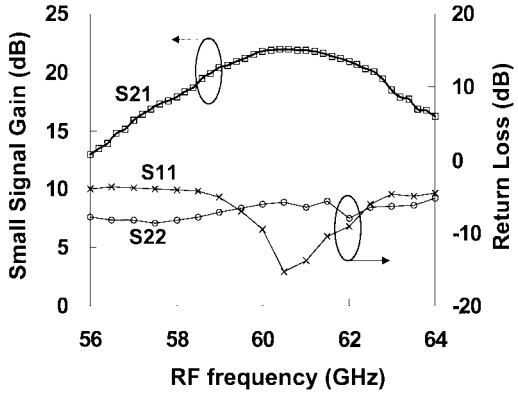

Fig. 10. Small-signal gain and the input and output return loss of the LNA.

The V-band oscillator is based on a parallel feedback topology and produced oscillation signals at 59.57 GHz. Design target frequency was 60 GHz. The output power was −1.6 dBm at 59.57 GHz and showed −109 dBc/Hz phase noise characteristics at a 10-MHz offset frequency. The photograph of the V-band oscillator is shown in Fig. 8. Fig. 9 shows the variation of the oscillation frequency and the output power as the control bias is changed from −1 to −0.6 V. The output power was −1.6 dBm ± 1.6 dB and the frequency tuning range was from 59.4 to 60 GHz. In order to provide enough LO signal power (∼3 dBm) to the mixer, a simple LO DA was also integrated in the package (not shown in Fig. 8).

A five-stage LNA was used in front of the mixer for gain and noise considerations. The LNA showed a gain higher than 20 dB at 59–62 GHz at the drain bias voltage of 2 V with a small bias current of 50 mA (Fig. 10). The four monolithic circuits were integrated in a WR-15 waveguide-based package together with the microstrip-to-finline-to-waveguide transitions. The loss of the finline transition was about 1.2 dB. The photograph of the V-band downconverter module is shown in Fig. 11. Fig. 12 shows the conversion gain of the whole package including the loss of interconnection between the chips as well as the loss of the transition. The LO frequency was fixed at 59.57 GHz. The overall gain of the integrated downconverter was higher than 20 dB over the RF bandwidth of 4.2 GHz (57.5∼61.7 GHz) without the IF amplifier. This result is among the highest RF conversion gain ever reported in this frequency range without the IF amplifier. The conversion gain of the downconverter

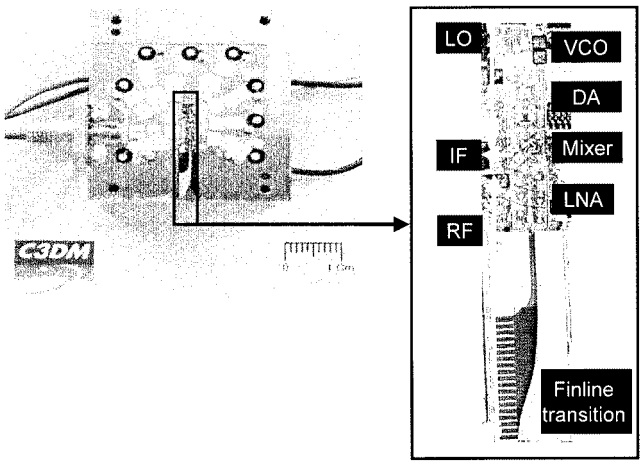

Fig. 11. Whole package photograph of the overall integrated V-band downconverter module.

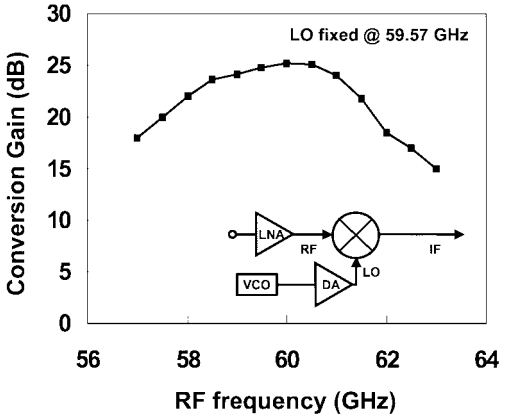

Fig. 12. Measured conversion gain of the integrated downconverter as a function of the RF frequency. The LO frequency is fixed at a 59.57 GHz.

started to roll off above 62 GHz due to the limited bandwidth of the LNA and the mixer.

V. Conclusion

High-performance V-band cascode pHEMT mixer and the downconverter module using the mixer chip were presented. The conversion gain and linearity of the cascode mixer were improved through the use of low-pass interstage circuits and bias optimization. The mixer achieved a high conversion gain of 6.3 dB. The IMD "sweet spot" theoretically predicted by the authors [1] was also observed from the V-band monolithic mixer chip. When tuned for linearity, the mixer showed an IP3 of 11.2 dBm together with a decent gain of 4.1 dB. A compact waveguide-based V-band downconverter module integrating the cascode mixer with an LNA, an LO amplifier, and a parallel feedback oscillator showed a high conversion gain over 20 dB from 57.5 to 61.7 GHz. This work demonstrates that a properly designed cascode mixer can be a promising candidate for compact downconverter applications at millimeter-wave frequencies.

Acknowledgment

The authors would like to thank S. Lee, K. Kang, and N. Kim, School of Electrical Engineering, Seoul National University, Seoul, Korea, for technical assistance during design, testing, and measurement.

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